

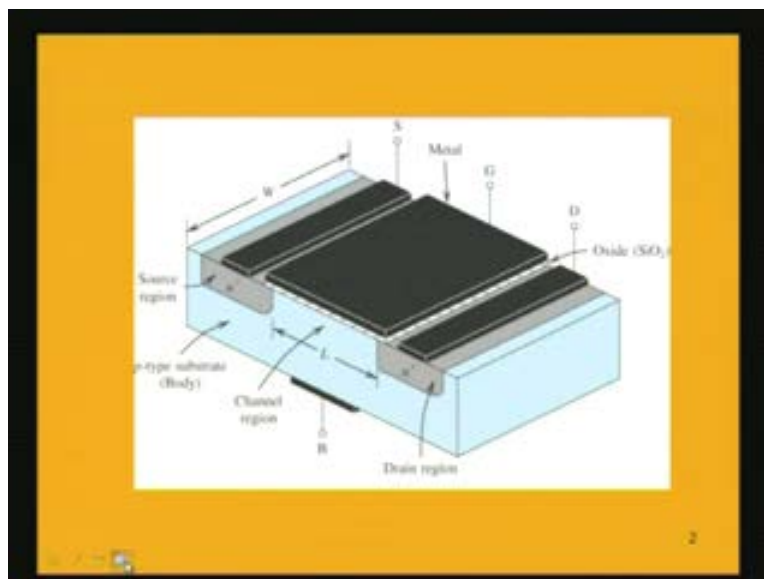
Basic Electronics
Prof. Dr. Chitralekha Mahanta
Department of Electronics and Communication Engineering
Indian Institute of Technology, Guwahati

Module: 3 Field Effect Transistors
Lecture-7
High Frequency Model of MOSFET Amplifier

In the last class we discussed about the small signal model of the MOSFET amplifier and we found out the amplifier parameters like input impedance, output impedance, voltage gain, etc using the small signal model. But one thing which is important and we ignored in the small signal model which we developed is that we ignored the capacitance effects. In fact there are capacitances present in the MOSFET device and we have to consider these capacitances when we want to see the frequency response. That means if we want to know about the gains when the frequency is low or very high then the capacitances have to be considered. Earlier also in BJT amplifiers we considered the junction capacitances which were present in the device and incorporating them into the small signal model we derived the $(\beta / (1 + \beta))$ model. Similarly here also in the MOSFET device because of the capacitance effects being present in the device we will have to consider these capacitances when we try to find out the frequency response that is the gain in the high frequency region and the low frequency region. The internal capacitances which are present in the MOSFET device are because of the structure of the device.

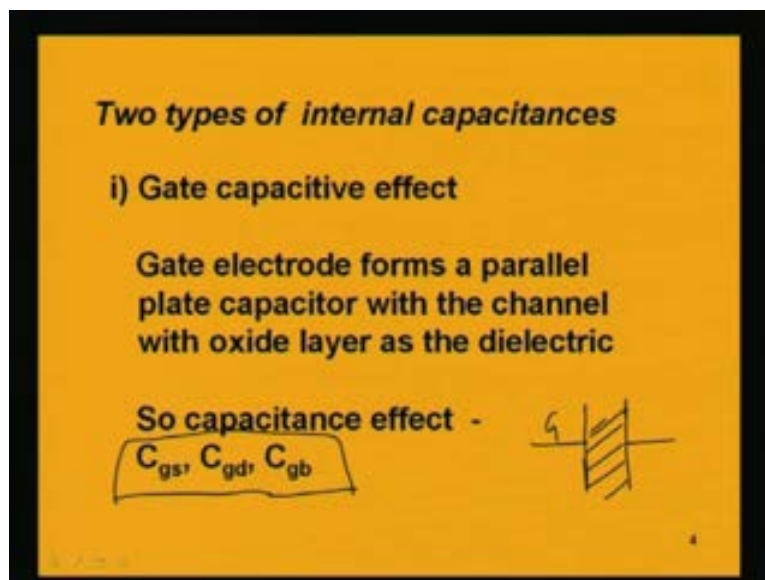
Let us see how the structure of the MOSFET device brings those capacitance effects. For that we will have to go back and see the physical structure once again. Let us recall the physical structure of the MOSFET device.

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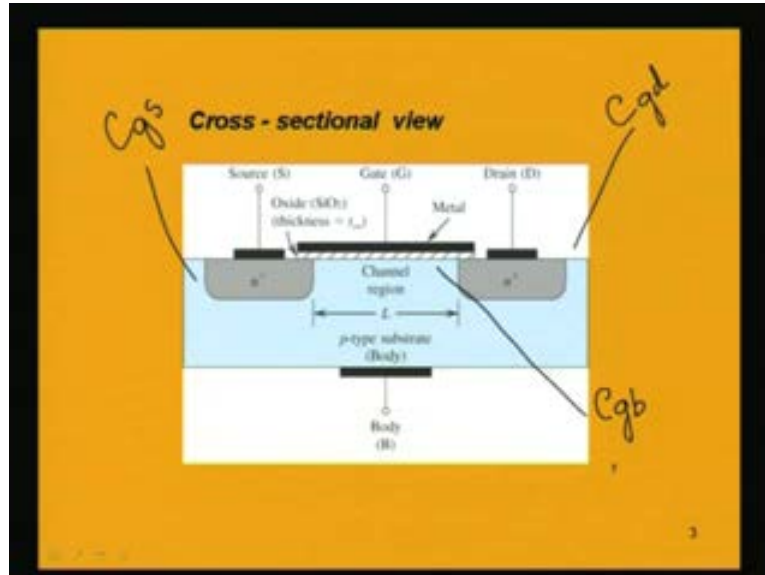
Here we have a silicon dioxide layer in between the gate and the substrate and this insulator which is present is basically forming a parallel plate capacitor between the gate and the body of the substrate. We know that between two parallel plates having insulator in between there will be a capacitance. Because this insulator having the dielectric is in between the gate and the substrate of the body, there will be capacitances between the gate and the source as well as the gate and the drain as well as the gate and the body. So we have three capacitances coming into existence because of the presence of this dielectric in between the gate and the substrate. Let us name these capacitances which are present between gate and the source, gate and the drain, and gate and the body as C_{gs} , C_{gd} and C_{gb} . These capacitances we will have to incorporate into the model which we have earlier derived.

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The three capacitances which are coming because of the gate is due to the gate electrode forming a parallel plate capacitor with the channel having oxide there, silicon dioxide in between them. It is like here, we are having this is the oxide layer in between the gate electrode and the body or the gate electrode and the channel. If we look into the whole channel, here this is the gate electrode and this is the source. In between them there is the oxide layer.

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Similarly this oxide layer is extending so it is forming a parallel plate capacitor between the gate and the channel. The channel is having these three regions; one is the drain, source and the body itself. In the region between the gate and the source because of this oxide layer there will be one capacitance here. That is C gate to source capacitance for this drain because from this gate electrode to this drain in between we have the oxide layer. That will be C gate to drain and from the substrate to the gate again there is this oxide layer so, that will be C gate to body. Apart from these three capacitances we have another type of capacitance and they are between the source and the body and the drain and the body because of the depletion layer.

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ii) Source-body and drain-body depletion-layer capacitances

- ❖ capacitance of the reverse- biased p-n junction formed by n-source and p-substrate : source diffusion
- ❖ capacitance of the reverse- biased p-n junction formed by n-drain and p-substrate : drain diffusion

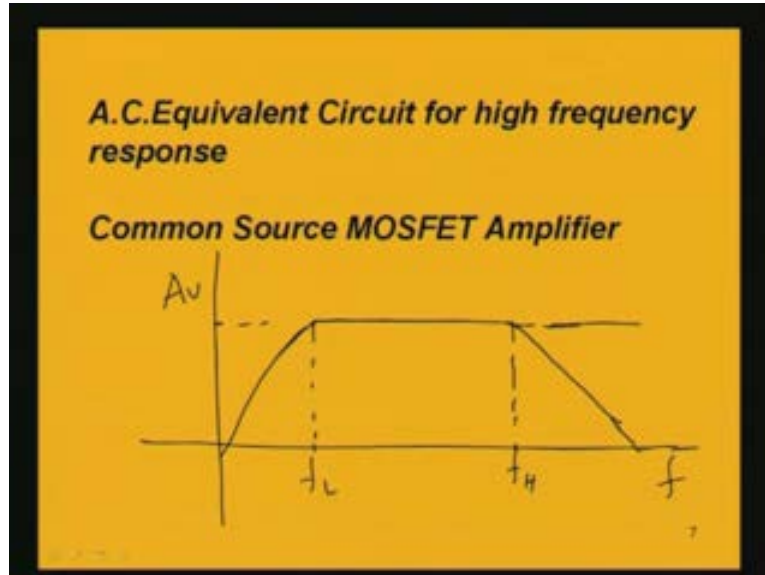
C_{sb}, C_{db}

If we look into the structure of this MOSFET device, there is a pn junction in between the source and the body because this body is made of p. We are considering a MOSFET device which is having a p-type substrate. It is an n-channel MOSFET we are considering. So, in between the source and the body, body means the substrate, we have a pn junction. Similarly drain is having a pn junction between the substrate and itself so, there are two pn junctions. These pn junctions will have the depletion layer capacitance and the depletion layer capacitance in the pn junction between the drain and the substrate or the body is known as drain diffusion. The pn junction depletion layer capacitance between the source and the substrate or the body is the source diffusion capacitance. Because of the presence of this depletion layer in the pn junction formed between the drain and the body as well as the source and the body, the drain diffusion and the source diffusion capacitances will be present. Because of the depletion layer capacitances we have two capacitances which are named as C_{sb} , source to body capacitance and C_{db} drain to body, C_{db} capacitance.

In all together we have now 5 capacitances which are the capacitances in the MOSFET device. We will have to consider these internal capacitances of the MOSFET device if we want to exactly draw the small signal model and this will be very important in order to know the response in the high frequency region because in the high frequency region these internal capacitances will be dominating. In the low frequency region also there will be capacitance effects but these capacitances are due to the coupling and by pass capacitors in the circuit. But these internal capacitances will affect the response when we consider the high frequency region. We have found earlier in the BJT amplifier that because of the capacitances being present in the amplifier circuit, we have a response. That means if we find out the gain versus frequency, it is not constant gain but it drops off in the low frequency and the high frequency regions. In the low frequency region the gain which you get in the mid band frequency region which is constant will drop off due to the external capacitances present in the circuit like coupling capacitor and the bypass capacitor.

In the high frequency region when we consider that the frequency of the signal being applied at the input is having a high frequency then the internal capacitances which we have just now described they will affect the gain. The gain will be reduced. In low frequency as well as high frequency region the gain of the amplifier drops off. We get a frequency response having a gain constant in the mid frequency region and in the high frequency and in the low frequency region it will drop off like this.

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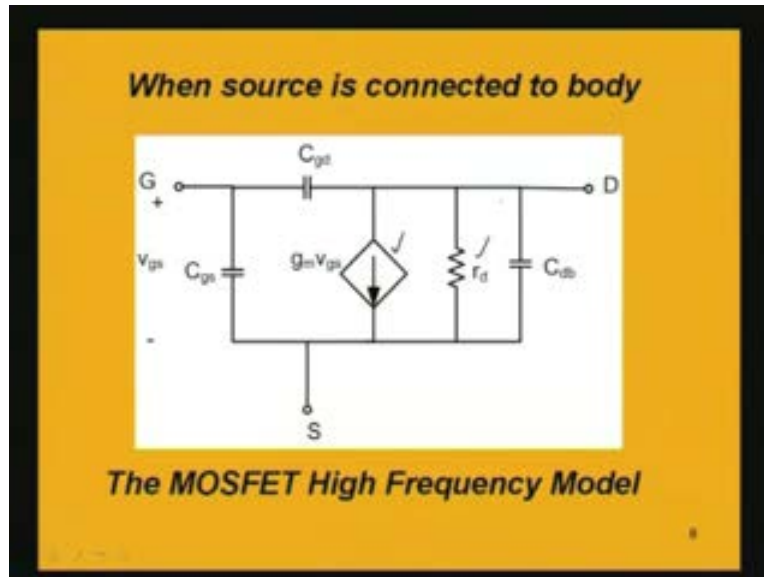


If we plot the gain versus frequency, if we suppose find out the voltage gain then at the mid band region the voltage gain will be constant. This is the mid band region and in the frequency when it is very low and very high it will drop off. This drop off is because of the capacitances which are present in the circuit in the low frequency region and because of the internal capacitances in the high frequency region. We know that there is 3dB frequency which is a very important one and that is when the gain drops up to $1/\sqrt{2}$ times the mid band gain, we get lower 3dB and higher 3dB frequencies. These two frequencies are cut off frequencies and all these considerations we have already discussed while discussing the BJT. Similar characteristics you will obtain here.

The small signal model which we will get when we consider these internal capacitances will be like in addition to those components which are in the small signal model we will have to augment by incorporating the internal capacitances. The small signal model components which are there or already we have derived; like we have the current source given by $g_m v_{gs}$ as well as the drain to source resistance are there. Apart from these components we will have now these capacitances which are the internal capacitances and we will have to incorporate these capacitances in the small signal model. Then we will get a pi model. We are going to draw that now. We already have this small signal model and in this small signal model these capacitances will be incorporated. But now we will consider 3 terminal device, which is mostly done in practical circuits. Three terminal MOSFET means we have the body and the source being connected. If the body and source is connected which results in a 3 terminal device then our job will be much simpler. The 5 capacitances which we have now got all these will not be applicable. Because the body and the source terminal is the same terminal they are connected. What will happen is that the source to body capacitance will simply vanish as well the gate to source and gate to body. These two capacitances will be only one capacitance from gate to source

We will get a small signal model when the source is connected to the body as shown here. We have this current source as well the r_d which we have already got in the small signal model which we discussed for the mid band gain.

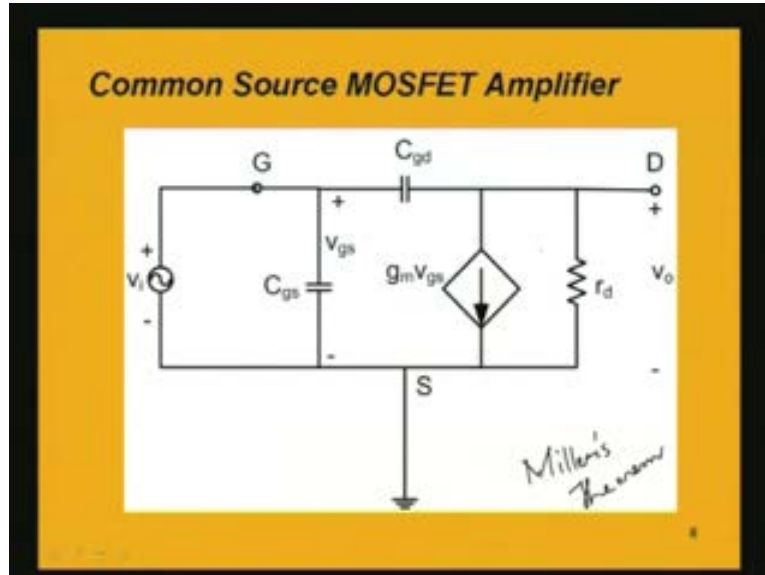
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We are having the gate to source capacitance. This is the capacitance from gate to source as is shown here. Then gate to drain capacitance that will be connected between gate and drain and there will be a drain to source or drain to body capacitance. Drain to body capacitance which we have seen because of the pn junction which is having the depletion layer, this capacitance between drain to body will be there. So we have extra 3 capacitances in the small signal model. We can further simplify by ignoring drain to body capacitance which is done in some books. Then we will have only the 2 capacitances gate to drain and gate to source. This model which is the high frequency model will be now plugged into the actual amplifier circuit and the response of the amplifier can be obtained. The computations etc, will be much complex now and it can be done easily in piece-wise, not manually because we are having now many computations to be performed.

If we now plug in this model into the amplifier circuit, draw the AC equivalent circuit for example for a common source MOSFET amplifier then the AC equivalent circuit for common source MOSFET amplifier will have these capacitances as shown here. For the time being we are now ignoring the drain to body capacitance.

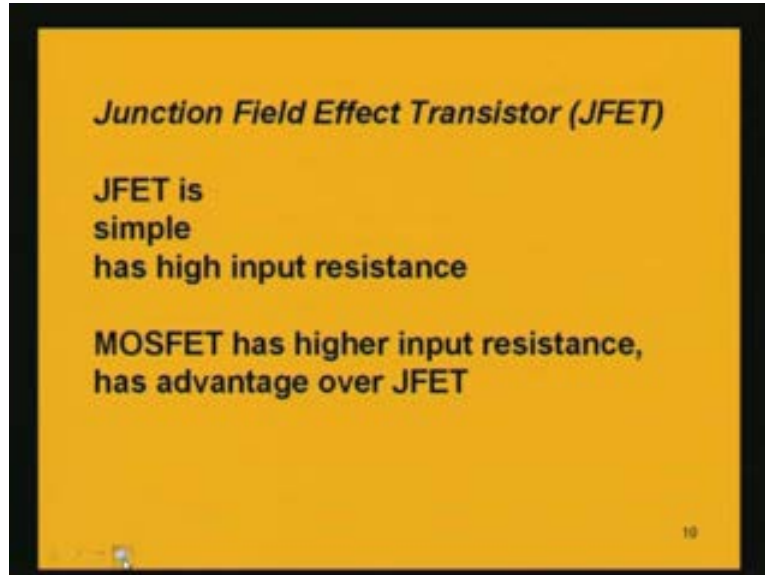
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Just for simplicity we are showing these two capacitances. If we look into this circuit which reminds us of the circuit that we considered for BJT amplifier in the high frequency response case, here actually we are having a capacitance between gate and drain, C_{gd} because of which this circuit is causing a problem for analysis. If we can somehow bring this capacitance in to either the input and output circuits or both by using some theorem then we will have easier analysis because then the input and output circuits will be isolated because this is the component which is the capacitance between gate and drain that is basically having a contact between the input and the output terminals. Here we will take help of the Miller's theorem. If you remember Miller's theorem what we used to do is that we were basically distributing this capacitance into input and output circuits. Then we will not have a capacitance in between gate and drain but we will have capacitance in the input and output circuits which can be combined with the capacitance which are already present. So that can be done and the analysis of the circuit will be following in a similar manner as we were earlier doing using Miller's theorem for BJT case. This Miller's theorem is used for finding the voltage gain. In the high frequency region you will find the voltage gain by using Miller's theorem to find the overall capacitance by distributing the capacitance C_{gd} , gate to drain capacitance bringing it to the input or the output side. This can be followed in a similar manner. Again we will not repeat that analysis here but this analysis can be easily followed as we have earlier done in BJT.

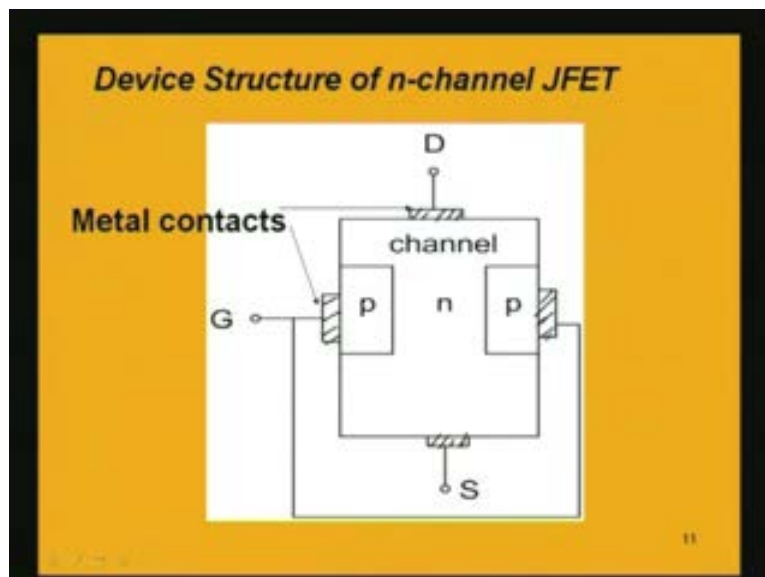
So far we have been discussing about the MOSFET device and this MOSFET device is having its name because we have seen in the construction that there is metal, there is oxide and semi conductor all are there in the device. There is another device which is also a field effect transistor or FET and it is the junction field effect transistor that is JFET. We will now discuss about the JFET. We have been discussing MOSFET. We have seen the enhancement type, depletion type MOSFET devices. JFET is also a field effect transistor; it is a simple FET device.

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It also has high input resistance because in MOSFET we have seen that the input resistance is very, very high. JFET is also a device which is having a high input resistance but this input resistance of the JFET is in fact less than the input resistance of the MOSFET and also there are some other advantages of the MOSFET device because of which actually the MOSFET is gaining popularity and this JFET is going to be obsolete day by day but still we will discuss JFET a little. Let us now see the structure of the JFET.

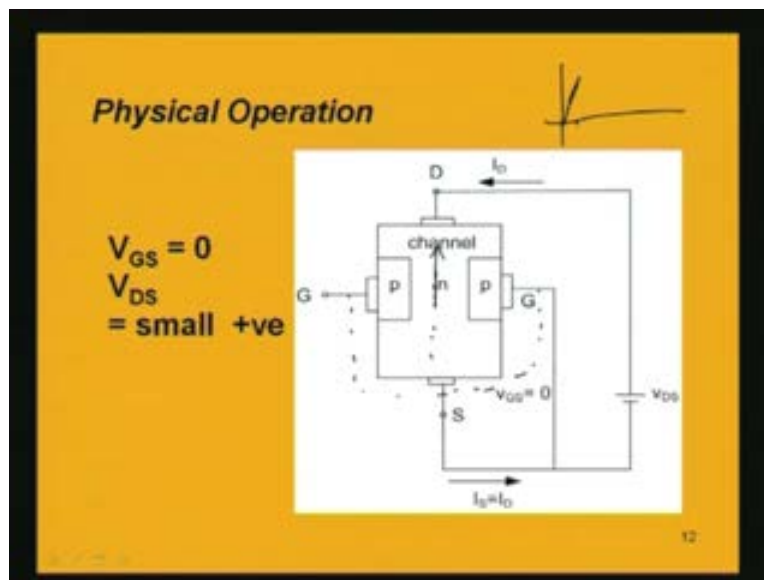
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The physical structure of the device is having n-channel that is a semiconductor which is n-type and there are two p-type semiconductors as shown in figure. There are metal contacts as shown here. These are the metal contacts and from these metal contacts we draw out three terminals which are known as the drain terminal, gate terminal and the source terminal as earlier in MOSFET device also we have got and here these two p's which are having the metal contacts are connected together. These two p's are connected together and a gate terminal is drawn out from these two metal contacts. We have the gate terminal which is having a contact with this p as well as this p. We can see that the same lead is connected to both the p through this metal contact and that is the gate terminal and there are drain and source terminal.

We are considering here an n-channel JFET. This is the channel which is the n-channel. This is the n-type semiconductor. In this structure as we can see here this is having n-type material which is rich in electron. So electrons will be abundant in this channel; n-channel it is and there are two p-type semiconductors. If we now apply a positive voltage V_{DS} that is we are having D, the drain at a positive potential with respect to the source and we do not apply any voltage between the gate and source. Then what will happen?

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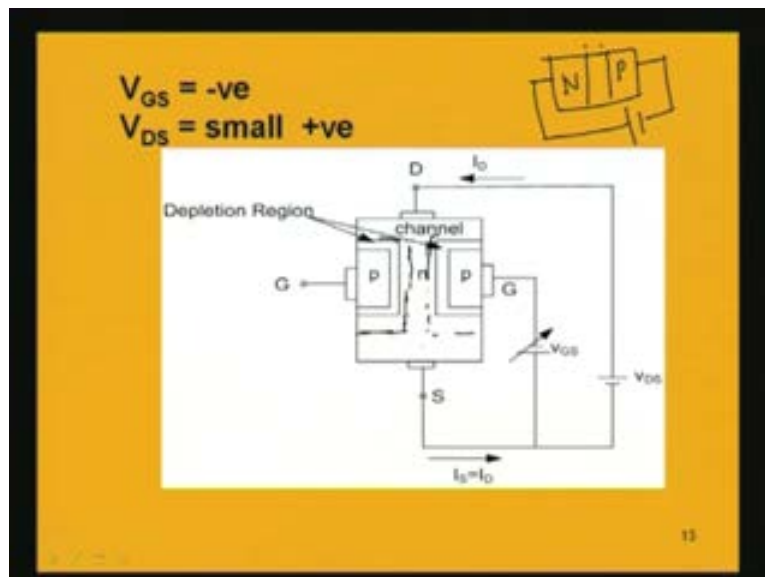
Suppose this is the condition where we are having no voltage between gate and source; only we are having positive voltage between drain and source and in order to simplify the diagram these two p-type materials which are connected to the gate, we are not showing this common connection. Actually there is a common connection between these two p's but instead of that we are just showing a gate terminal here also. It means that this is also a gate terminal because these two p's are connected by these two metal contacts and this lead is connecting these two metal contacts. These two p's are having the same gate terminal which is described by writing G here. This is also G; this is also G.

We are not applying any gate to source voltage that means gate to source voltage is now zero. There is no potential being applied between the gate and source terminal. But there is a positive potential at the drain with respect to the source. What will happen is that if we apply the V_{DS} positive, V_{DS} has to be kept at a low voltage; we should not increase the V_{DS} because if we go on increasing the V_{DS} that will have another effect which we will discuss later. Right now let us assume that we are applying a small positive voltage between drain and source and gate to source voltage is zero. That is simply like gate to source terminal is being short circuited. Because of the abundance of the electrons present in the n-channel, these are electrons present; they will be attracted by the positive terminal of this V_{DS} . So there will be a flow of a current between drain and source.

The conventional direction of the current is from top to bottom, from drain to source as shown in this arrow mark. As electrons are moving from source to drain in this direction so the current direction is opposite to it which is the conventional direction of current that is the drain current it is called; it is from drain to source. The same current will now go out from the source terminal and ending at the negative terminal of the V_{DS} . This completes the current part. The drain current is equal to the source current. It is clear that we are not applying any gate to source voltage. Even then the current will flow from drain to source because of the attractive force due to the V_{DS} on the electrons in the channel. We are keeping this V_{DS} small. When it is very small the current will be small but as we increase a little it will be like an ohmic contact; like in ohmic device current increases linearly. Initially if V_{DS} is small, for the smaller region when we increase a little it will increase the current. Then if we go on increasing the V_{DS} then another phenomenon will occur which is the saturation or pinching off. That we will discuss.

Next let us apply a negative potential between gate and source.

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If we are having a gate to source voltage which is negative, drain to source voltage is positive. What will happen there is a depletion layer between the p and n as well as this p and n. This depletion layer, depletion region or depletion layer, will be dependent upon the reverse voltage being applied. Which one is the reverse voltage? We are having a negative voltage between gate and source, V_{GS} . By this variable arrow mark we are meaning that we are changing the V_{GS} that is gate to source voltage is varying. Initially it was zero; what we have seen earlier. Now it has increased a little. If we go on increasing what will happen to the width of the depletion region? It will increase because as far as this p and n is concerned we are having this gate to source voltage negative; p is connected to negative and this n is connected to positive. So this is a reverse biasing voltage. Due to this reverse biasing voltage if we increase this voltage this depletion region will increase.

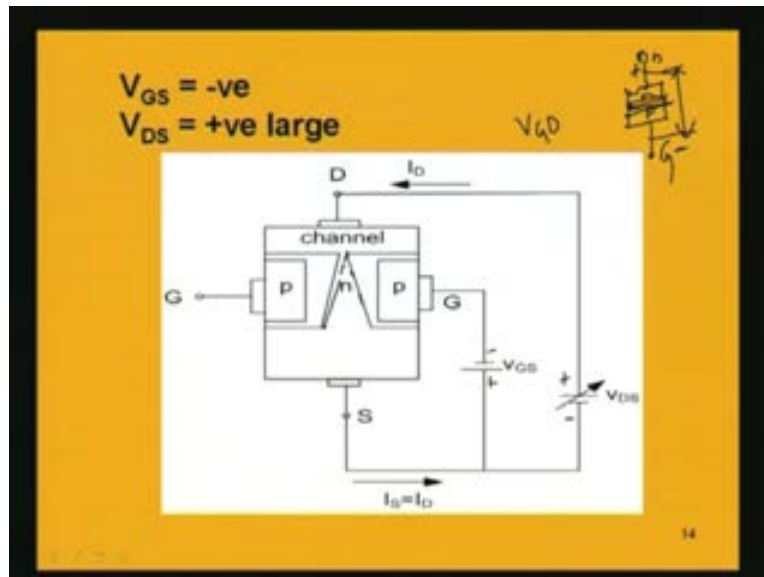
In between the p and n region whatever depletion region is there, depletion layer, which is the region where you have the immobile charges only that region will increase if we increase the reverse biasing voltage; that we already know. When this depletion region increases here also it will increase to a broader depletion region. Here it will also be increasing to a broader level. Then what will happen is that the channel width will be narrower and narrower. Width of the channel is narrower means the drain current will go on decreasing because the drain current is dependent up the charge carriers present in the channel. The channel is narrowing down means lesser charge carriers will be now available to flow. So the current between drain and source will reduce. If we go on increasing the V_{GS} then at a point what will happen is that the channel will be totally bereft of charge carriers and the current will be zero. That voltage between the gate and source in the negative region or the negative gate to source voltage at which the drain current becomes zero is called the pinch off voltage. It is like the threshold voltage in the depletion type MOSFET.

In the depletion type MOSFETs also we have seen that there is a threshold voltage below which the gate to source potential should not go because then the current will be zero. Similarly here this pinch off voltage is that voltage between the gate to source. It is negative, mind it. At that voltage the drain current becomes zero. In order to have a drain current flowing we must have gate to source voltage greater than the pinch off voltage. So every JFET device will have its pinch off voltage specified. If you go on varying gate to source voltage then the current will go on reducing and reducing and it will become zero when it reaches the pinch off voltage. Mind it we are not changing the drain to source voltage. The drain to source voltage is constant. Basically what is happening is that the gate to source voltage is having a control on the drain current, the control being effected via the gate to source voltage. When we have this gate to source voltage negative we are having a hold over the drain current because drain to source voltage is not changed. It is constant voltage we are applying. What will happen if we keep gate to source voltage constant and vary the drain to source voltage?

Next let us discuss that situation when we have a constant negative gate to source voltage but drain to source voltage is now varied. Drain to source voltage is having the polarity as

shown here. This is positive this is negative. That means drain is at a positive potential with respect to the source.

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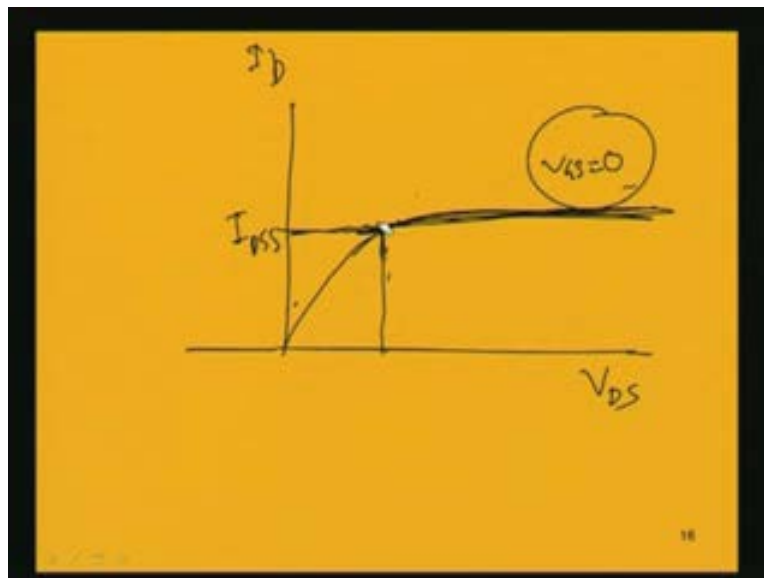
What will happen now is that initially when we have a smaller drain to source voltage, the current will increase along with the increase of drain to source voltage almost in a linear region because now it is like an ohmic device. The n-channel resistance will define the current and you go on increasing. When the V_{DS} is small an increase of V_{DS} will give more force on the electrons in n-channel. So current will increase. But then if we go on increasing the V_{DS} to a high value what will happen is that the channel between these two p's that n-channel which is present, this n-channel will have a change in its width. Because one phenomenon which is happening here is that the depletion region which is present in the p-n diode that is in between the p-n materials, this depletion region is dependent upon the reverse biasing voltage. As we increase the V_{DS} , the reverse biasing voltage which is present between the gate and the drain will change. When we have a small V_{DS} then whatever was the region in the depletion layer that will be not same when you increase the V_{DS} . Because increasing the V_{DS} means that the reverse biasing potential for this p-n diodes or the p-n materials will now increase towards the drain side, if you go on increasing V_{DS} because gate to drain potential is dependent upon this drain to source potential.

Gate to drain potential is important because on that the width of the depletion layer will depend. If we go on increasing V_{DS} too much then the depletion layer width will increase and increase and the n-channel will have a modulation in its width. It will taper towards the drain side. That is the width will be maximum at the source side and it will taper or narrow down towards the drain side because at the drain side the reverse biasing potential for this pn is maximum. This is due to too much increment in the V_{DS} . What will happen is that if we go on increase V_{DS} a point will be reached when the n-channel will have only a point of touch at the drain side. It will be almost like it will be touching at the drain

side; it will be like this. When this happens it is also like a pinching off phenomenon. There will be saturation of the drain current and that is why when we go on increasing the drain to source voltage, the drain current will reach a point of saturation or pinching off and beyond that even if you go on increasing the drain to source voltage, the current will remain constant at the saturation value. This phenomenon is similar to the pinching off that we discussed in MOSFET.

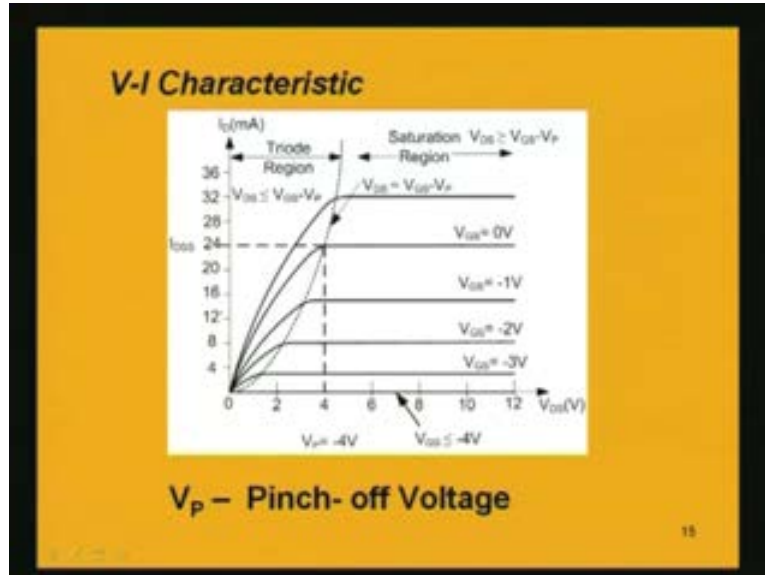
It is due to this reverse biasing potential between gate and drain being varied because of the variation in V_{DS} . If you look into the two terminals gate and drain which are having the n and p, the drain is having this channel n. This drain is having this n and this gate is having this p. So the depletion layer depends upon the potential between the gate and drain. The drain is positive gate is negative. That means we have now V_{GD} which is basically the determining factor. Because of this phenomenon happening in this JFET for variation in V_{GS} as well as variation in V_{DS} keeping one constant at a time we can now draw the VI characteristic. One thing to notice that when V_{GS} was zero the current which is flowing between drain and source due to the presence of the small positive voltage between drain and source V_{DS} , saturating value of that current is known as I_{DSS} . I_{DSS} is the current which is the maximum current or the saturating or the pinching off current that is flowing in the device when we have gate to source voltage zero. Because of this phenomenon of pinching off what is happening is here if we go on increasing the V_{DS} a point will be reached when we have the saturation or pinching off. Suppose at this point it is pinching off. This maximum current I_D is known as I_{DSS} for V_{GS} is equal to zero. This is the I_{DSS} . This current I_{DSS} has the maximum value for this V_{GS} is equal to zero and you have in JFET device this is specified; I_{DSS} will be specified.

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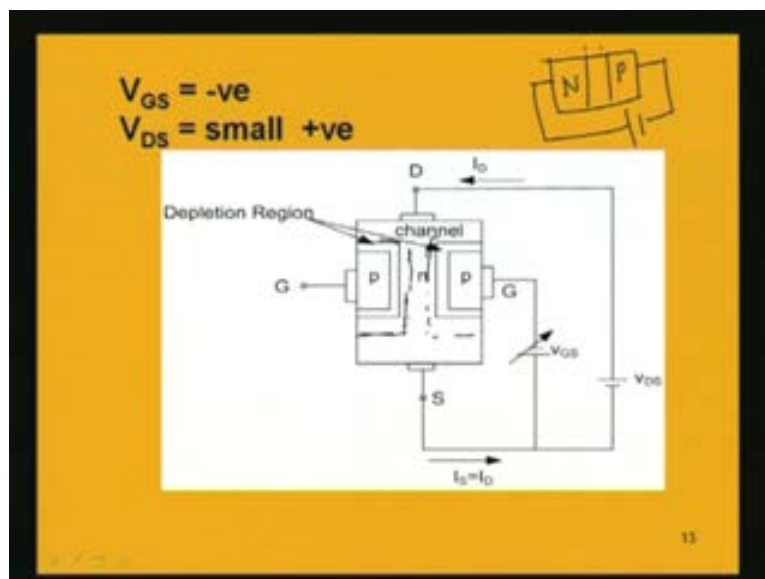
In order to draw the VI characteristic we have to map all these regions like as we have done in the MOSFET. For JFET device here these regions are as you can see here V_{DS} is positive and this is the corresponding I_D .

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For different values of gate to source voltage starting from zero to negative we are plotting this. Here one point that is important here is that you cannot apply V_{GS} positive. Because in this JFET if we have V_{GS} positive we are applying suppose a gate to source voltage positive then the current will not be controlled by the gate to source voltage. The gate to source voltage will loose its control over the drain current. Now visualize that this gate and source is having a positive voltage.

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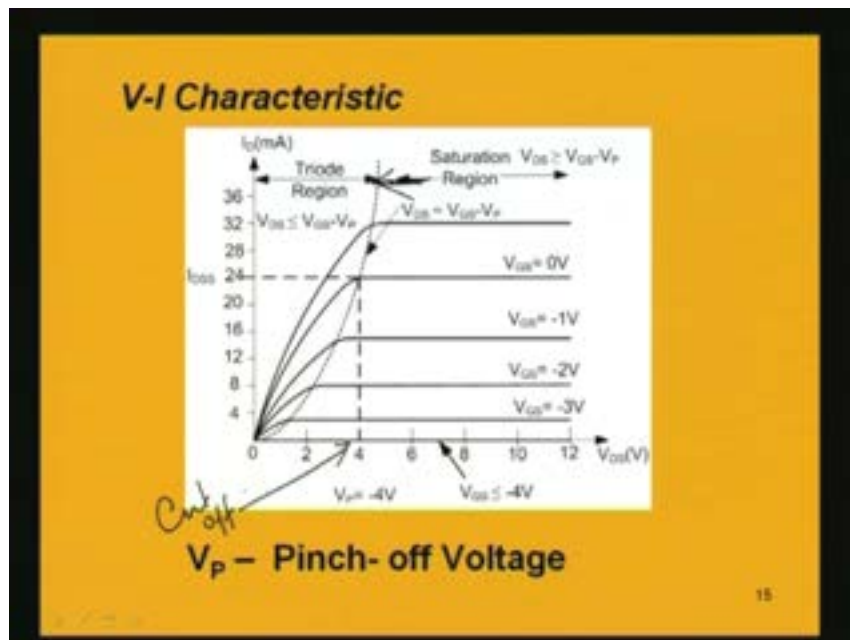
It is p; it is n. This is positively connected. That means current will increase and it cannot be controlled. Only when V_{GS} is negative it has a hold over the drain current because by

modulation of the depletion layer in the p-n, the current is controlled. Unlike depletion type MOSFET, which had the depletion region as well as enhancement region, where we could keep V_{GS} positive also that is not possible for this JFET device. It is only operated when V_{GS} is negative and a maximum value of V_{GS} you can give is zero. We cannot give positive voltage. That means we cannot go beyond V_{GS} is equal to zero.

Now the V-I characteristic can be plotted by mapping all these regions into the I_D versus V_{DS} curve and as we have discussed when the magnitude of V_{GS} is less than the pinch off voltage, then drain current will be zero. This is the line because here for this example we are taking that pinch off voltage is equal to -4 volt. If V_{GS} is less than -4 volt then the drain current will be zero and that is shown by this line, the line which is just coinciding with the zero line under V_{DS} axis. That is the cut off region. That is called cut off region. The device is turned OFF. Now we have V_{GS} is equal to zero. Then we get this curve. This is the maximum current that is the saturating current when V_{GS} is equal to zero and that is known as the I_{DSS} current. This is the drain to source current when V_{GS} is equal to zero. If we go on increasing the V_{GS} say V_{GS} is equal to -1 volt, -2 volt, -3 volt, this way then the current will reduce and reduce. Because of the depletion region being increased the channel width being reduced so, the drain to source current will be reduced. That is reflected in this plot that the drain current will reduce if you go on reducing the V_{GS} . That can be seen here.

When we reach the pinch off voltage by reducing the gate to source voltage then we get totally zero current and if we now increase the drain to source voltage as we have seen here the current will reach the pinching off or saturation region. In this region is the saturation region. This is the saturation region where we have the condition that drain to source voltage is higher than gate to source voltage minus pinch off voltage.

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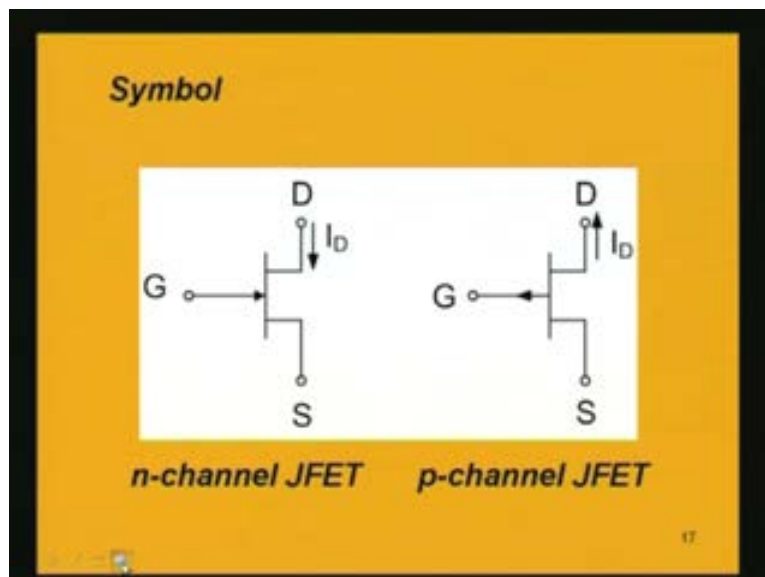


Here also it reminds you of the depletion type MOSFET. There the condition for the saturation of the drain to source current was when the drain to source voltage was greater than gate to source voltage minus the threshold voltage and that threshold voltage has a counterpart here which is the pinch off voltage. Otherwise it is the same characteristic and when we have these two voltages equal then this is the locus of these points when V_{DS} is equal to V_{GS} minus V_p . This curve is actually plotted from the points of the saturation that is when the saturation point is reached. As we go on increasing the V_{GS} from say bottom to top we are going, then the saturation is shifted towards right and right; at a more voltage the saturation is happening. When the drain source to voltage is less than V_{GS} minus V_p , pinch off voltage this region is known as the triode region. We have cut off then triode, then saturation region; these three regions.

One important thing as we have mentioned is that V_{GS} cannot be positive. We do not have an enhancement region as we were having in depletion type of MOSFET. In depletion type of MOSFET, we were having two regions; depletion as well as enhancement. But the JFET does not have the enhancement region means we do not have the region when V_{GS} is equal to positive; that is not possible. This characteristic curve give us the idea about how we can control the drain to source current by changing the gate to source voltage in the negative way. If we apply a negative voltage between gate to source we can control the drain to source current. If we go on increasing the gate to source voltage, the drain to source current will go on reducing.

Next we draw the symbol for the JFET.

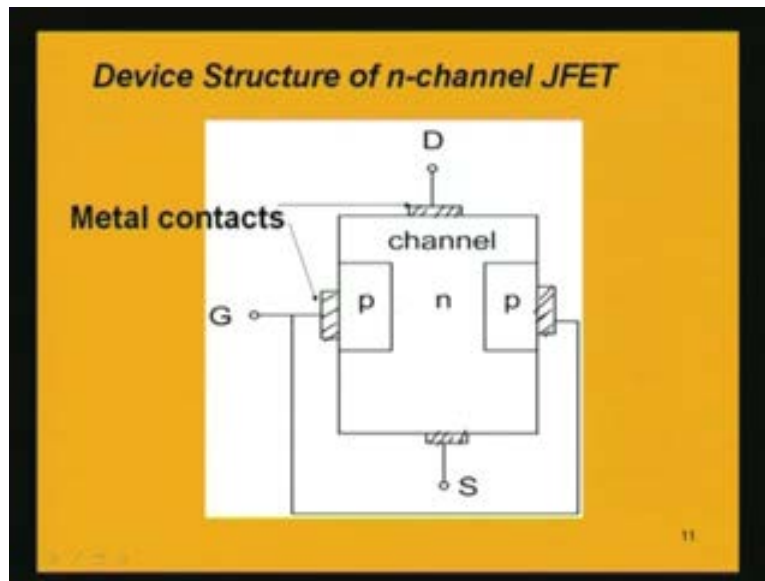
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This is the symbol. We have two different types of JFET; n-channel and p-channel. n-channel is having the channel made of n and two p-type. Similarly in the p-channel, the channel will be made of p and there will be two n-type regions. The symbol is as shown here for the n-channel and this is for the p-channel. The drain current direction will be

reverse for the p-channel because accordingly we will apply the polarities there in the p-channel. The direction of the arrow from the gate is actually indicative of the direction of the current in the channel. If it is n-channel, the current will be from the p region to the n region. The gate will have a direction of current as shown here because if we look into the device structure this is p and this is n.

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From p to n current flows. That is indicative of the arrow head in the gate terminal. Similarly if it is a p-channel that means the channel is made of p. So you will have current from p to the gate. p to n means p to the gate. These two are symbolic representations for the two types of JFET and it is meaningful in that way, that you can know whether the channel is n or p by simply looking at the arrow. The current which flows in the device from drain to source, this I_D current is given by an important equation known as Shockley's equation. This is Shockley's equation which relates the current with the voltages. This equation gives you the value of the drain current which is given by I_{DSS} into $1 - \frac{V_{GS}}{V_P}$ whole squared. V_{GS} is the gate to source voltage and V_P is the pinch off voltage. It will be whether V_{GS} negative or positive and we have seen that generally we will have only negative voltage because V_{GS} is always given a negative voltage and pinch off voltage also has to be negative voltage.

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In saturation (pinch-off) region

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Shockley's Equation

I_{DSS}, V_P

The current equation can be used for finding out one another important parameter which is the trans-conductance g_m . Here this I_{DSS} and V_P , these two are important parameters for the particular JFET device under use. That means if we are using a JFET device you must know the value of pinch off voltage and the I_{DSS} current. This will be generally given in the data sheet. Whatever JFET device you are using that will have the values of the pinch off voltage and the I_{DSS} written in the data sheet. These two are known for a particular JFET device, which we are using. If we know these two depending upon what gate to source voltage we are applying we can find out the drain to source current for that gate to source voltage. It is a square which signifies the non-linearity of the curve. It is not a straight line or it is not having a straight line equation. It is having a non-linear equation given by this square term and that is very obvious. We could see in the plot of current versus voltage that it is a non-linear curve only. The value of I_D depends on I_{DSS} and now if we consider the drain to source voltage, the drain to source voltage should be such that it will make the JFET device current or I_D current in saturation. It will be in saturation and the saturation region is generally used for amplification like we have seen in MOSFET.

Today we have discussed about one important phenomenon in MOSFET device which was the small signal model having the internal capacitances which are coming because of the construction of the MOSFET device and because of the internal capacitances being present in the MOSFET device from gate to channel as well as from drain to body and source to body we have to consider these capacitances and incorporate in the small signal model. Using this pi model or the small signal model having the capacitances we can find the high frequency response and the voltage at the high frequency will reduce than the mid band voltage gain what we studied in BJT also. Next we have started discussion on FET device, which is the junction field affect transistor. We have seen the V-I characteristic and next we will discuss how to use this JFET in actual amplifier.